UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR DUAL TAPERING AN OPTICAL WAVEGUIDE

Inventors: Ansheng Liu
Doron Rubin

Prepared By:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025-1026
(206) 292-8600

Attorney's Docket No.: 42P17910

"Express Mail" mailing label number:
Date of Deposit:EV320118510US
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to addressed to Mail Stop Patent Application, Commissioner for Patents, Alexandria, VA 22313-1450
Luci M. Arevalo
(Typed or printed name of person mailing paper or fee)
Luci M. Arevalo
(Signature of person mailing paper or fee)
November 13, 2003
(Date signed)

METHOD AND APPARATUS FOR DUAL TAPERING AN OPTICAL WAVEGUIDE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to optics and, more specifically, the present invention relates to optical waveguide tapers.

Background Information

The need for fast and efficient optical-based technologies is increasing as Internet data traffic growth rate is overtaking voice traffic pushing the need for optical communications. Transmission of multiple optical channels over the same fiber in the dense wavelength-division multiplexing (DWDM) systems and Gigabit (GB) Ethernet systems provide a simple way to use the unprecedented capacity (signal bandwidth) offered by fiber optics. Commonly used optical components in the system include wavelength division multiplexed (WDM) transmitters and receivers, optical filter such as diffraction gratings, thin-film filters, fiber Bragg gratings, arrayed-waveguide gratings, optical add/drop multiplexers, lasers and optical switches.

Many of these building block optical components can be implemented in semiconductor devices. As such, these devices are typically connected to an optical fiber and it is therefore important to obtain an efficient coupling of light between the fiber and the semiconductor device containing the optical components. Light is typically propagated through the optical fibers and optical waveguides in semiconductor devices as a single mode. Three-

dimensional tapered waveguides or mode size converters are important to realize efficient light coupling between a single mode fiber and a single mode semiconductor waveguide device because semiconductor waveguide devices usually have smaller mode sizes compared to optical fiber mode sizes. This is usually because of the large index contrast of semiconductor waveguide systems and the required smaller waveguide dimensions for the device performance such as high speed in a silicon based photonic device.

Previous attempts at three-dimensional tapered waveguides or mode size converters include various tapering schemes and fabrication methods that are for example based on gray scale lithography technology, which requires a complicated etch process. Other attempts include taper methods that are difficult to combine with the electrically active photonic device processes, which typically involves many back-end process steps.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures.

Figure 1 is an illustration of one embodiment of a dual taper waveguide device including a buried tapered waveguide and a tapered rib waveguide in accordance with the teachings of the present invention.

Figure 2 is a side view diagram of one embodiment of a dual taper waveguide device illustrating a mode of an optical beam propagating through the buried tapered waveguide being directed up and into a slab portion of a tapered rib waveguide adjoining the buried tapered waveguide in accordance with the teachings of the present invention.

Figure 3 is a cross section view of one embodiment of a larger or input end of a dual taper waveguide device in accordance with the teachings of the present invention.

Figure 4 is a cross section view of one embodiment of a smaller or output end of a dual taper waveguide device in accordance with the teachings of the present invention.

Figure 5 is a top view diagram illustrating one embodiment of three different masks used when fabricating a dual taper waveguide in accordance with the teachings of the present invention.

Figure 6 is a side view diagram illustrating one embodiment of a silicon-on-insulator (SOI) wafer during fabrication of a dual taper waveguide device in accordance with the teachings of the present invention.

Figure 7 is a side view diagram illustrating one embodiment of an SOI wafer during fabrication of the dual taper waveguide device after a first semiconductor layer is etched with a first mask in accordance with the teachings of the present invention.

Figure 8 is a side view diagram illustrating one embodiment of an SOI wafer during fabrication of the dual taper waveguide device after a second semiconductor layer is etched with a second mask in accordance with the teachings of the present invention.

Figure 9 is a front view diagram illustrating the tip of one embodiment of a dual taper waveguide device in an SOI wafer during fabrication of the dual taper waveguide device after the second semiconductor layer is etched with the second mask in accordance with the teachings of the present invention.

Figure 10 is a side view diagram illustrating one embodiment of an SOI wafer during fabrication of a dual taper waveguide device after an insulating layer is grown in accordance with the teachings of the present invention.

Figure 11 is a front view diagram of the sharpened tip of one embodiment of a dual taper waveguide device in an SOI wafer during fabrication of the dual taper waveguide device after the second semiconductor layer is etched with the second mask in accordance with the teachings of the present invention.

Figure 12 is a side view diagram illustrating one embodiment of an SOI wafer during fabrication of a dual taper waveguide device after epitaxial lateral overgrowth (ELO) silicon is grown in accordance with the teachings of the present invention.

Figure 13 is a front view diagram illustrating the sharpened tip of one embodiment of an SOI wafer during fabrication of a dual taper waveguide device after the ELO silicon is grown in accordance with the teachings of the present invention.

Figure 14 is a front view diagram illustrating a smaller end of a tapered rib waveguide formed during fabrication of a dual taper waveguide device after the tapered rib waveguide has been patterned in accordance with the teachings of the present invention.

Figure 15 is a block diagram illustration of one embodiment of a system including one embodiment a semiconductor device including a dual taper waveguide device and a photonic device according to embodiments of the present invention.

DETAILED DESCRIPTION

Methods and apparatuses reducing or converting a mode size of an optical beam with a dual taper waveguide device are disclosed. In the following description numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments. In addition, it is appreciated that the figures provided herewith are for explanation purposes to persons ordinarily skilled in the art and that the drawings are not necessarily drawn to scale.

In one embodiment of the present invention, a novel dual taper waveguide that can be used to efficiently couple light between single mode fiber and a silicon photonic device is disclosed. The taper process can be

completed according to embodiments of the present invention before photonic device processes in a semiconductor layer and therefore, back-end process compatibility problems are reduced.

In one embodiment of the present invention, a semiconductor-based dual taper waveguide device is provided in a fully integrated solution on a single integrated circuit chip. As illustrated in Figure 1, one embodiment of a dual taper waveguide device 101 disposed in semiconductor material in accordance with the teachings of the present invention includes a buried tapered waveguide 105 adjoining a tapered rib waveguide 107. The tapered rib waveguide 107 includes a slab portion 109 and a rib portion 111. As shown in Figure 1, an optical beam 103 is directed into a larger end 113 of dual taper rib waveguide. In one embodiment, the mode size of optical beam 103 has a mode size such that portions of optical beam 103 propagate through both buried tapered waveguide 105 and tapered rib waveguide 107 when entering dual taper waveguide device 101 at the larger end 113.

In one embodiment, the slab portion 109 of the tapered rib waveguide 107 adjoins the buried tapered waveguide 105 such that the buried tapered waveguide 105 is adapted to direct the mode of the portion of the optical beam 103 propagating through the buried tapered waveguide 105 into the slab portion 109 of the tapered rib waveguide 107. Therefore, the mode size of optical beam 103 is reduced such that substantially all of optical beam 103 with the reduced mode size is output from dual taper waveguide device 101 from the smaller end 115 of tapered rib waveguide 107.

In one embodiment, optical beam 103 is received at the larger end 113 of dual taper waveguide device 101 from an optical fiber and optical beam 103 is then directed from the smaller end 115 of dual taper waveguide device 101 to a photonic device disposed in the same semiconductor material layer as dual taper waveguide device 101 such that dual taper waveguide device 101 is provided in a fully integrated solution on a single integrated circuit chip.

Figure 2 is a side view diagram of one embodiment of a dual taper waveguide device 101 illustrating the size of a mode of an optical beam 103 propagating through dual taper waveguide device 101 being reduced when being directed from a larger end 113 of the dual taper waveguide device 101 to the smaller end 115 of the dual taper waveguide device 101. As shown, dual taper waveguide device 101 includes a buried tapered waveguide 105, which in one embodiment is fabricated as a two-dimensional taper buried in a semiconductor layer of a silicon-on-insulator (SOI) wafer in accordance with the teaching of the present invention. In one embodiment, dual taper waveguide device 101 further includes a tapered rib waveguide 107, which in one embodiment is fabricated as a two-dimensional tapered waveguide adjoining buried tapered waveguide 105. In one embodiment, tapered rib waveguide 107 includes a rib portion 111 and a slab portion 109, as illustrated above for example in Figure 1, which is adjoining buried tapered waveguide 105 in accordance with the teachings of the present invention.

As the shown in the depicted embodiment, the mode of the portion of optical beam 103 propagating through buried tapered waveguide 105 is pushed or directed into tapered rib waveguide 107 as optical beam 103 propagates along buried tapered waveguide 105. In one embodiment, the mode of optical beam 103 that is directed from buried tapered waveguide 105 is directed into the slab portion of tapered rib waveguide 107. As such, the mode size of optical beam 103 is reduced such that substantially all of optical beam 103 is directed out the smaller end 115 of dual taper waveguide device 101 through tapered rib waveguide 107.

To illustrate, Figure 3 is a cross section view of one embodiment of the larger end 113 of dual taper waveguide device 101 in accordance with the teachings of the present invention. As shown, the intensity distribution of optical beam 103 is such that it is propagated through both buried tapered waveguide 105 and tapered rib waveguide 107 at larger end 113.

Figure 4 shows a cross section view of one embodiment of the smaller end 115 of dual taper waveguide device 101 in accordance with the teachings of the present invention. In one embodiment, the rib portion 111 of tapered rib waveguide 115 at smaller end 115 is reduced in size, as shown in Figure 4, when compared to rib portion 111 of tapered rib waveguide 115 at larger end 113, as shown in Figure 3. The buried tapered waveguide 105 at smaller end 115 is reduced in size to a sharp tip, as shown in Figure 4, when compared buried tapered waveguide 105 at larger end 113, as shown in Figure 3. As shown in the embodiment depicted in

Figure 4, the portion of the mode of optical beam 103 originally propagating through buried tapered waveguide 105 has been directed or pushed up from buried tapered waveguide 105 into tapered rib waveguide 107 through rib portion 109 at smaller end 115.

Accordingly, the mode size of optical beam 103 has been reduced with dual taper waveguide device 101 in accordance with the teachings of the present invention.

In one embodiment, the tip width at the smaller end 115 of buried tapered waveguide 105 is fabricated to be as small or sharp as possible in accordance with the teachings of the present invention, which is typically determined by the lithographic resolution and etch process. In one embodiment, the tip width at the smaller end 115 of buried tapered waveguide 105 can be made even sharper or smaller by including an insulating layer in the semiconductor material layer, which will be described in greater detail below, in accordance with the present invention.

To illustrate, top view illustrations of the masks used to fabricate a dual taper waveguide device 101 are shown in Figure 5. Three masks are illustrated in Figure 5, the first of which is mask 501, which is the largest. Mask 503 is used when fabricating buried tapered waveguide and mask 505 is used when fabricating the rib portion 111 of tapered rib waveguide 107.

As shown in the depicted embodiment, mask 503 is shaped such that buried tapered waveguide 105 will have the length of L_0. In addition, mask 503 is shaped such that buried tapered waveguide 105 will have first and

second taper regions. The first taper region of buried tapered waveguide 105 will taper at a first taper rate from the width of W_0 to a width of W_2 over a length of L_1. In the second taper region of buried tapered waveguide 105, the buried tapered waveguide 105 will taper at a second rate from a width of W_2 to a sharp point over a length of L_2. In one embodiment, the width of the sharp point is determined in part by the lithographic resolution and etch process. As shown in the embodiment depicted in Figure 5, the first and second taper rates are different. For example, in one embodiment, W_0 is approximately 10 μm, W_2 is approximately 3 μm and L_1 is approximately 100-200 μm for the first taper region. In the second taper region, the buried tapered waveguide 105 will taper at a second rate from approximately 3 μm to the sharp point over approximately 1.3-1.4 mm. In one embodiment, the total length L_0 is approximately 1.5 mm.

With regard to mask 505, it is shaped such that the rib portion 111 of tapered rib waveguide 107 will also have a length of L_0 and shaped such that tapered rib waveguide 105 will have first and second taper regions. The first taper region of the rib portion 111 of the tapered rib waveguide 107 will taper at a first taper rate from the width of W_0 to a width of W_1 over the length of L_1 and the second taper region will taper at a second rate from the width of W_1 to a width of W_3 over the length of L_2. In one embodiment, W_1 is slightly larger than W_2 and W3 is approximately 1.8-1.9 μm.

In one embodiment, it is noted that a relatively short taper length is used for the first taper region, when the dual waveguide taper device 101 for

example tapers from for example 10 μm to 3 μm, and a longer taper is used for the second taper region because both horizontal and vertical mode conversion occurs in the second taper region and the optical radiation loss of the dual taper waveguide device 101 in one embodiment depends on the taper length. By including the first and second taper regions with different taper rates, dual taper waveguide device 101 is shorter compared to other taper devices with a single taper rate. As a result, dual taper waveguide device 101 is able to reduce the size of the mode with less radiation loss compared to other longer tapers. In one embodiment, simulation results have shown that a small taper loss of only approximately 0.26 dB can be obtained with an embodiment of a dual taper device 101 having an approximately 1.5 mm taper length tapering from approximately 10 x 10 μm to approximately 1.8 x 1.9 μm in accordance with the teachings of the present invention.

It is appreciated that the specific dimensions and taper rates illustrated herewith are provided for explanation purposes and that other dimensions or rates may also be utilized in accordance with the teachings of the present invention.

Figures 6 through 14 are diagrams illustrating one embodiment of a process to fabricate a dual taper waveguide device 101 in accordance with the teachings of the present invention. In particular, Figure 6 is a side view diagram illustrating one embodiment of a silicon-on-insulator (SOI) wafer 601 during fabrication of a dual taper waveguide device 101 in accordance

with the teachings of the present invention. As shown, wafer 601 includes a first semiconductor layer 603, a buried insulating layer 605 and a second semiconductor layer 607. In one embodiment, first and second semiconductor layers 603 and 607 include silicon and buried insulating layer 605 includes an oxide.

In the embodiment shown in Figure 7, the first semiconductor layer 603 is etched away using mask 501, as shown for example in Figure 5, as a mask. As shown, an opening 701 is formed in semiconductor material layer 503 down to buried insulating layer 605. In one embodiment, mask 501 is a relatively large rectangular mask and therefore enables opening 701 to provide access to buried insulating layer 605 to later etch an opening for buried tapered waveguide 105.

Figure 8 shows a side view of wafer 601 after buried insulating layer 605 and second semiconductor layer 607 are etched using the mask 503, as shown for example in Figure 5, to form an opening 801 for the buried tapered waveguide 105. In the embodiment depicted in Figure 8, the larger end 113 of the dual taper waveguide device 101 will be on the left hand side of the diagram and the smaller end 115 will be on the right hand side.

Figure 9 is a front view diagram illustrating one embodiment of a cross section of wafer 601 at the tip or smaller end 115 of where dual taper waveguide device 101 will be formed in accordance with the teachings of the present invention. It is noted that views of the openings 701 and 801 formed by the masks 501 and 503, respectfully, can be better appreciated in

Figure 9. In the embodiment shown in Figure 9, the tip or smaller end 115 of the opening 801 for the buried tapered waveguide 105 has a width of T_1. In one embodiment, T_1 is the critical dimension (CD) or is the minimum width possible for the lithographic process used to etch opening 801. For example, in one embodiment, T_1 is approximately 1.135 μm.

Figure 10 shows a side view of wafer 601 after an insulating layer 1001 is grown in the opening 801 formed previously. In one embodiment, insulating layer 1001 includes oxide and is grown to a thickness of approximately 0.5 μm thick. As such, insulating layer provides vertical as well as horizontal confinement of an optical beam propagating through buried tapered waveguide 105 in accordance with the teachings of the present invention.

Figure 11 is a front view diagram illustrating one embodiment of a cross section of wafer 601 at the tip or front end 115 after the insulating layer 1001 is grown in the opening 801 in accordance with the teachings of the present invention. As can be noted in the embodiment depicted in Figure 11, the tip or smaller end 115 of the opening 801 for the buried tapered waveguide 105 now has a width of only T_2 after the insulating layer 1001 is grown. As a result, the tip or smaller end 115 of the opening 801 has been sharpened or reduced in size from T_2, as illustrated in Figure 8 to T_1 by growing insulating layer 1001 in accordance with the teachings of the present invention. In one embodiment, T_2 has a width of only approximately 0.206 μm. Therefore, by growing insulating layer 1001, relatively low-cost

and low-resolution lithography tools may be utilized to create a sharp tip at the smaller end of the opening 801. Moreover, the sharpness of the tip can receive critical dimensions that are beyond conventional lithography capabilities in accordance with the teachings of the present invention.

Figure 12 is a side view diagram illustrating one embodiment of wafer 601 after semiconductor material 1201 is grown in and over the opening 801 and the insulating layer 1001. In one embodiment, semiconductor material 1201 includes epitaxial lateral overgrowth (ELO) silicon. In one embodiment, the material of semiconductor material 1201 will be the core material of the buried tapered waveguide 105 and the tapered rib waveguide 107 of the dual taper waveguide device 101 in accordance with the teachings of the present invention.

Figure 13 is a front view diagram illustrating one embodiment of a cross section of wafer 601 at the tip or front end 115 after the ELO silicon of semiconductor material 1201 is grown in accordance with the teachings of the present invention. As can be appreciated from the depicted embodiment, the tip or front end 115 of buried tapered waveguide 105 is sharp as defined by insulating layer 1001. Tapered rib waveguide 107 will be adjoining buried tapered waveguide 105 from above, as illustrated in the embodiment depicted in Figure 13.

In one embodiment, after semiconductor material 1201 is grown, it is then polished and then the rib portion 111 of tapered rib waveguide 107 is then patterned using mask 505, as illustrated in Figure 5. To illustrate,

Figure 14 provides an illustration of one embodiment of a front view diagram of the cross section of wafer 601 at the tip or front end 115 after tapered rib waveguide 107 is then patterned using mask 505 in accordance with the teachings of the present invention. As can be appreciated from the depicted embodiment, the rib portion 111 and slab portion 109 are now defined in the ELO silicon of semiconductor material 1201. The slab portion of 109 of tapered rib waveguide 107 is adjoining buried tapered waveguide 105 from above as shown. It is noted that the cross section view of dual taper waveguide device 101 at the larger end 113 is as it appears and is described above in Figure 3.

Figure 15 is a block diagram illustration of one embodiment of a system 1501 including one embodiment a semiconductor device including a dual taper waveguide device and a photonic device according to embodiments of the present invention. As illustrated in the depicted embodiment, system 1501 includes an optical transmitter 1505 to output an optical beam 1505. System 1501 also includes an optical receiver 1509 and an optical device 1507 is optically coupled between the optical transmitter 1503 and optical receiver 1509. In one embodiment, the optical device 1507 includes semiconductor material, such as for example a silicon layer in a chip, with a dual taper waveguide device 1509 and a photonic device 1511 included therein. In one embodiment, dual taper waveguide device 1509 is substantially similar to dual taper waveguide device 101 described in Figures 1-13 above. In one embodiment, dual taper waveguide

device 101 and photonic device 1511 are semiconductor-based devices that are provided in a fully integrated solution on a single integrated circuit chip.

In operation, optical transmitter 1503 transmits optical beam 1505 to optical device 1507 through an optical fiber 1513. Optical fiber 1513 is then optically coupled to optical device 1507 such that optical beam 1507 is received at an input to dual taper waveguide device 1509. In one embodiment, the input to dual taper waveguide device 1509 corresponds to the larger end 113 of dual taper waveguide device 1509. Accordingly, with dual taper waveguide device 1509, the mode size of optical beam 1505 is reduced in sized such that a photonic device 1511 receives optical beam 1505 through a single mode waveguide 1517 disposed in the semiconductor material of optical device 1507. In one embodiment, photonic device 1511 may include any known semiconductor-based photonic optical device including for example, but not limited to, an optical phase shifter, modulator, switch or the like. After optical beam 1505 is output from photonic device 1511, it is then optically coupled to be received by optical receiver 1509. In one embodiment, optical beam 1505 is propagated through an optical fiber 1515 to propagate from optical device 1507 to optical receiver 1509.

In the foregoing detailed description, the method and apparatus of the present invention have been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit

and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.